National Cheng Kung University, Tainan, Taiwan
IEEE Circuits and Systems Society, Tainan Chapter

Design Trade-Offs in Digital Intensive PLLs

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Time: 6/12, 10 AM
Venue: 成功大學電機系館 靄雲廳

Abstract

The speech will give a comprehensive overview and provide an intuitive understanding of digital PLLs in spatial domain. Operating principles and limitations of digital PLLs are demonstrated by introducing an architecture-independent model with numerical calculations in the time domain. Various digital PLL architectures, including all-digital and hybrid PLLs are presented. Finally, all-digital self-calibration techniques and digitally-assisted PLLs are discussed.

Biography

Ping-Ying Wang received the M.S. degree in physics science from National Taiwan University, Taipei, Taiwan, in 1994. From 1999 to 2003 he worked at Etron and Realtek, Taiwan, developing all-digital PLLs and spread-spectrum clocking. In 2003, He joined Mediatek, Taiwan, where he developed all-digital CDR for high-speed serial links, hybrid PLLs and all- digital self-calibration techniques for PLL-based modulators. From 2010 to 2014, he was technical director for the Mixed-Signal Design Division working on all-digital regulation techniques and all-digital charge pumps for PLLs. Currently, he is co-founder of a company, CMOS-Crystal, focused on PLLs integrated with crystal amplifiers. He holds over 36 granted patents, and has published over 23 peer-reviewed journal and conference papers. He serves on the IEEE International Solid-State Circuits Conference DCT subcommittee.